WHAT IS CLAIMED IS

1. A high-performance apparatus for data conversion, comprising:

a. a conversion unit that includes at least two lower-performance converters, each said converter having at least one lower performance parameter than the high-performance apparatus for data conversion, said conversion unit operative to convert an input signal obtained in a time domain;

b. a processing unit coupled to said conversion unit and operative to process frequency domain information extracted from said input signal, and, based on said processed frequency domain information, operative to provide in combination with said conversion unit at least two processed signals; and

c. a recombining unit operative to combine said at least two processed signals into a single high-performance output signal.

2. The apparatus of claim 1, wherein said processing unit includes:

i. a transform unit operative to perform on said input signal a transform from said time domain to a frequency domain to provide a frequency domain input signal,

ii. a frequency domain information extraction unit operative to perform said extraction through a division of said frequency domain into at least two frequency domain parts, one said part related to a low-resolution signal to noise ratio (SNR) and the other said part related to a high-resolution SNR, and

iii. a processor operative to process said frequency domain information.

3. The apparatus of claim 2, wherein each of said at least two lower performance converters is an analog-to-digital converter, wherein said input signal is an analog input signal, wherein one of said at least two processed signals is a first processed digital signal jointly processed by a first of said analog-to-digital converters (ADC1) and by said processing unit, and wherein a second of said processed signals is a second processed digital signal jointly processed by a second of said analog-to-digital converters (ADC2) and by said processing unit.

4. The apparatus of claim 3, further comprising

d. a subtractor operative to subtract an analog subtraction signal processed by said processor from said analog input signal, said subtractor providing an analog error signal that is further converted by said ADC2 into an ADC2 output signal.

5. The apparatus of claim 4, wherein said transform unit includes a digital transform unit operative to perform said transform and to provide said frequency domain input signal, wherein said frequency domain information extraction unit includes a spectral analysis unit operative to perform said division of said frequency domain into at least an upper frequency domain part and a lower frequency domain part by identifying said upper frequency domain part with a threshold, and wherein said processor includes:

A. a digital filtering unit operative to perform digital filtering of frequencies below said threshold and to provide a first digitally filtered output,

B. an inverse transform function operative to inversely transform said first digitally filtered output back into a first filtered time domain digital signal, and

C. a first digital-to-analog converter (DAC1) operative to convert said first filtered time domain digital signal into said analog subtraction signal.

6. The apparatus of claim 4, wherein said transform unit includes a digital transform unit operative to perform said transform and to provide said frequency domain input signal, wherein said frequency domain information extraction unit includes a spectral analysis unit operative to perform said division of said frequency domain into at least an upper frequency domain part and a lower frequency domain part by identifying said upper frequency domain part with a threshold, and wherein said processor includes:

A. a digital filter operative to filter an output signal received from said ADC1 and to output an output filtered signal with strongly attenuated below-threshold frequencies, and

B. a first digital-to-analog converter (DAC1) operative to convert said output filtered signal into said analog subtraction signal.

7. The apparatus of claim 4, further comprising:

e. a calibration/equalization unit operative to calibrate said recombining unit.

8. The apparatus of claim 7, wherein said processor further includes a post-DAC filtering unit operative to filter analog subtraction signal prior to its input to said subtractor, said post-DAC filtering providing a further improvement in the high-performance of the apparatus.

9. The apparatus of claim 4, wherein said transform unit includes a digital transform unit operative to perform said transform and to provide said frequency domain input signal, wherein said frequency domain information extraction unit includes a spectral analysis unit operative to perform said division of said frequency domain into at least an upper frequency domain part and a lower frequency domain part by identifying said upper frequency domain part with a threshold, and wherein said processor includes:

A. a digital filtering unit operative to perform digital filtering of frequencies below said threshold and to provide a first digitally filtered output,

B. an inverse transform function operative to inversely transform said first digitally filtered output back into a first filtered time domain digital signal, and

C. a subtraction signal synthesizer operative to synthesize said analog subtraction signal from frequency domain information.

10. The apparatus of claim 6, wherein said transform unit includes a first Fast Fourier Transform (FFT1) function operative to perform said transform and provide said frequency domain input signal, wherein said frequency domain information extraction unit includes a spectral analysis unit operative to perform said division of said frequency domain into at least an upper frequency domain part and a lower frequency domain part by identifying said upper frequency domain part with a threshold, and wherein said processor includes:

A. a first spectral window filter operative to perform digital filtering of frequencies below said threshold and to provide a first digitally filtered output,

B. a first inverse Fast Fourier Transform (IFFT1) function operative to inversely transform said first digitally filtered output back into a first filtered time domain digital signal, and

C. a first digital-to-analog converter (DAC1) operative to convert said first filtered time domain digital signal to provide said analog subtraction signal.

11. The apparatus of claim 10, further comprising:

e. a second Fast Fourier Transform (FFT2) function operative to perform a transform from the time domain to the frequency domain on said ADC2 output signal to provide an FFT2 output signal;

f. a second spectral window filter operative to perform digital filtering of frequencies above said threshold and to provide a second digitally filtered output

g. a digital summer for recombining said first and second digitally filtered outputs and for providing an FFT sum output, and

h. a second inverse Fast Fourier Transform (IFFT2) function operative to inversely transform said FFT sum output into a second filtered time domain digital signal.

12. The apparatus of claim 1, wherein said recombining unit includes a digital spectral combining unit operative to provide an optional frequency domain digital output and a transform-to-time unit operative to provide a time domain digital output.

13. A high-resolution, high-speed apparatus for data conversion, comprising:

a a first, low-resolution analog-to-digital converter (ADC1) operative to output a first digital output signal in a time domain;

b. a first spectral signal processor operative to use a frequency domain to both convert said first digital output signal into an output analog subtraction signal and to provide a processed digital signal;

c. a second low-resolution analog-to-digital converter (ADC2) operative to convert an analog error signal formed in a subtraction operation involving said output analog subtraction signal into a second digital output signal; and

d. a digital combining unit operative to receive said processed digital signal and said second digital output signal and to combine both said signals into a final digital output signal;

whereby the apparatus has a higher resolution that either said ADC1 or said ADC1, and

whereby the data conversion is performed in the frequency domain using spectral tools, thereby providing an improved dynamic range and quantization noise, a reduction or elimination of critical analog circuit requirements and bottlenecks, and an increase of the sampling rate relative to existing pipeline/subranging architectures.

14. The apparatus of claim 13, further comprising:

e. a splitter connected to said ADC1 and operative to split an input analog signal into a main channel analog signal used in said subtraction operation and a secondary subtraction channel analog signal input to said ADC1, said main channel analog signal fed to said ADC1.

15. The apparatus of claim 14, further comprising:

f. a subtractor operative to perform said subtraction operation; and

g. a delay inserted in a path between said splitter and said subtractor and operative to compensate for delays occurring in said subtraction channel.

16. The apparatus of claim 13, wherein said digital combining unit includes a digital spectral combining unit operative to provide an optional frequency domain digital output, and a transform-to-time unit operative to provide a time domain digital output.

17. The apparatus of claim 15, further comprising:

h. an amplitude scaling unit coupled to said ADC2 and operative to adapt said analog error signal to a range of said ADC2;

i. a separate optional digital combining unit operative to combine said first and second digital output signals of respectively said ADC1 and ADC2 and to output an optional digital signal; and

j. at least one optional second spectral signal processor coupled to said ADC2 and to said digital combining unit and operative to provide at least one additional subtraction stage.

18. The apparatus of claim 13, wherein said first spectral signal processor includes:

i. a transform function operative to transform said first digital output signal from said time domain to said frequency domain, thereby providing a first transformed digital signal;

ii. a spectral analysis unit operative to perform spectral analysis in said frequency domain using said first transformed digital signal and to provide output frequency information that includes a dynamic frequency range divided into above-threshold frequencies and below-threshold frequencies;

iii. a digital filtering unit operative to strongly attenuate said below-threshold frequencies and to transfer without attenuation said above-threshold frequencies to provide a digitally filtered output;

iv. an inverse transform function operative to inversely transform said digitally filtered output into an inversely transformed output; and

v. a first digital-to-analog converter (DAC1) operative to receive and convert said output frequency information and said inversely transformed output into said output analog subtraction signal.

19. The apparatus of claim 18, wherein said first spectral signal processor further includes a post-DAC analog filtering unit coupled to said subtractor and operative to filter said output analog subtraction signal prior to its input to said subtractor.

20. The apparatus of claim 18, wherein said transform function is performed by a Fast Fourier Transform (FFT) and wherein said inverse transform function is performed by an Inverse Fast Fourier Transform (IFFT).

21. The apparatus of claim 18, wherein said transform function is performed by a filter bank.

22. The apparatus of claim 13, wherein said first spectral signal processor includes:

i. a transform function operative to transform said first digital output signal from said time domain to said frequency domain, thereby providing a first transformed digital signal;

ii. a spectral analysis unit operative to perform spectral analysis in said frequency domain using said first transformed digital signal and to provide output frequency information that includes a dynamic frequency range divided into above-threshold frequencies and below-threshold frequencies, each said above-threshold frequencies and below-threshold frequencies including respective spectral peaks;

iii. a digital filter operative to filter an output signal received from said ADC1 and to output a filtered signal with strongly attenuated below-threshold frequencies, and

iv. a first digital-to-analog converter (DAC1) operative to convert said output filtered signal into said output analog subtraction signal, and

v. a post DAC filter operative to attenuate said below-threshold frequencies, thereby providing additional improvement of quantization noise and errors of said DAC1.

23. The apparatus of claim 13, wherein said first spectral signal processor includes:

i. a transform function operative to transform said first digital output signal from said time domain to said frequency domain, thereby providing a first transformed digital signal;

ii. a spectral analysis unit operative to perform spectral analysis in said frequency domain using said first transformed digital signal and to provide output frequency information that includes a dynamic frequency range divided into above-threshold frequencies and below-threshold frequencies;

iii. a digital filtering unit operative to strongly attenuate said below-threshold frequencies and to transfer without attenuation said above-threshold frequencies to provide a digitally filtered output;

iv. a plurality of inverse transform functions operative to inversely transform said digitally filtered output into separate respective inversely transformed outputs; and

v. a subtraction signal synthesizer that synthesizes above-threshold frequency signals from said respective inversely transformed outputs

24. The apparatus of claim 14, further comprising a calibration/equalization unit operative to calibrate said apparatus.

25. The apparatus of claim 24, further comprising:

f. a signal conditioner operative to condition said secondary subtraction channel analog signal before its input to said ADC1, and

g. a transform function operative to receive said second digital output signal from said ADC2 and to transform said second digital output signal from said time domain to said frequency domain, thereby obtaining a second transformed digital signal in the frequency domain.

26. A method for implementing a high-performance converter comprising the steps of:

a. processing a frequency domain signal and a time domain input signal using at least two data converters having each at least one lower performance parameter than the high-performance converter in order to obtain at least two processed signals, wherein said processing includes:

i. transforming said time domain input signal into said frequency domain signal in a digital form,

ii. dividing said frequency domain into at least two frequency domain parts, a first said part related to a low-resolution signal to noise ratio (SNR) and a second said part related to a high-resolution SNR thereby extracting frequency domain information from said frequency domain signal in a digital form, and

iii. using said frequency domain information to obtain said at least two processed signals; and

b. recombining said at least two processed signals to obtain a first final output signal from the high-performance converter;

whereby the method provides higher performance and other advantages than comparable data conversion methods that work in the time domain.

27. The method of claim 26, wherein said dividing of said frequency domain into at least two frequency domain parts includes providing a threshold above said low-resolution SNR, said threshold determining said division, thereby providing above-threshold frequencies in a window W1 and below-threshold frequencies in a window W2, said W! and W2 correlated respectively with said first and seconds frequency domain parts.

28. The method of claim 27, wherein said time domain input signal is an analog signal, wherein said high-performance converter is a high-performance analog-to-digital converter (ADC), wherein a first of said at least two lower performance converters is a first high-speed, low-resolution analog-to-digital converter (ADC1), and wherein said transforming further includes using said ADC1 to convert a subtraction channel representation of said time domain analog input signal into a first time domain digital output signal which is fed to a first spectral processor.

29. The method of claim 28, wherein a second of said at least two lower performance converters is a second analog-to-digital converter (ADC2), wherein said step of transforming is preceded by a step of splitting said analog input signal into a main channel signal representation and into said subtraction channel signal representation, both said signals representing said analog input signal, and wherein said step of processing further includes:

i. using said first spectral processor to process said first time domain digital output signal and to obtain above-threshold frequency information in a digital form; and

ii. generating, by said first spectral processor and using said above-threshold frequency domain part, a first digitally filtered output signal and an analog subtraction signal, said analog subtraction signal subtracted in a subsequent subtraction operation from said main channel signal, said subtraction operation providing an analog error signal.

30. The method of claim 29, wherein said step of recombining said at least two processed signals to obtain a final output signal from said high-performance ADC converter includes:

i. processing said analog error signal formed in said subtraction operation,

ii. converting said error signal into a second digital output signal using said ADC2, and

iii. digitally combining said first digitally filtered output signal and said second digital output signal into a first final digital output signal, using a first digital combining unit.

31. The method of claim 27, wherein said time domain input signal is a digital signal, wherein said high-performance converter is a high-performance digital-to-analog converter (DAC) having both high-resolution and high-speed, wherein a first of said at least two lower performance converters is a DAC with the same high-speed but lower resolution than said high-performance DAC while all the rest of said at least two lower performance DAC are lower-speed, high-resolution DACs, and wherein said transforming includes directly transforming said input signal from said time domain into said frequency domain.

32. The method of claim 31, wherein said step of recombining includes parallel frequency interleaving of said at least two processed analog signals.

33. The method of claim 27, wherein said step of recombining said at least two processed signals to obtain a final output signal from the high-performance converter includes obtaining a first final digital output signal in a domain selected from the group consisting of a time domain and a frequency domain.

34. The method of claim 30, further comprising the step of coupling a second spectral processor to said ADC2 and said first digital combining unit to provide at least one additional subtraction stage.

35. The method of claim 30, further comprising the step of combining said first digital output signal from said ADC1 and said second digital output signal from said

ADC2 in a second digital combining unit to optionally provide a second final digital output in a time domain.

36. The method of claim 30, wherein said dividing of said frequency domain into at least two frequency domain parts is performed using a spectral analysis unit included in said first spectral processor, wherein said generating of a digitally filtered output signal is performed by a digital filtering unit coupled to said spectral analysis unit and wherein said generating of an analog subtraction signal is performed by a digital-to-analog converter coupled to said digital filtering unit through an inverse transform function.

37. The method of claim 29, wherein said step of recombining said at least two processed signals to obtain a final output signal from said high-performance ADC converter includes:

i. processing said analog error signal formed in said subtraction operation,

ii. converting said error signal into a second digital output signal using said ADC2,

iii. transforming said second digital output signal into a second frequency domain signal,

iv. digitally filtering said second digital frequency domain signal by passing all said below-threshold frequencies and strongly attenuating all said above-threshold frequencies in a second spectral window filter to obtain a second digitally filtered output signal, and

v. summing vectorially said first and second digitally filtered output signals to provide a frequency domain digital output signal.

38 The method of claim 29, wherein said step of recombining said at least two processed signals to obtain a final output signal from said high-performance ADC converter includes:

i. processing said analog error signal formed in said subtraction operation,

ii. converting said error signal into a second digital output signal using said ADC2,

iii. transforming said second digital output signal into a second frequency domain signal,

iv. digitally filtering said second digital frequency domain signal by passing all said below-threshold frequencies and strongly attenuating all said above-threshold frequencies in a second spectral window filter to obtain a second digitally filtered output signal,

v. equalizing said second frequency domain signal and subtracting the result of said equalization from said first digitally filtered output signal in said W1 frequency range to obtain an improved resolution first digitally filtered output signal;

vi. summing vectorially said improved resolution first digitally filtered output signal and said second digitally filtered output signal to provide a frequency domain digital output signal, thereby obtaining better resolution within an .FFT bin

39. A method for implementing a high-performance analog-to-digital converter comprising the steps of:

a providing a first, low-resolution analog-to-digital converter (ADC1) operative to convert an analog input signal into a first digital output signal in a time domain;

b. providing a first spectral signal processor operative to process said first digital output signal and other received digital signals in a frequency domain and to provide a processed digital signal;

c. providing a second low-resolution analog-to-digital converter (ADC2) operative to convert an analog error signal formed in a subtraction operation involving said output analog subtraction signal into a second digital output signal; and

d. providing a digital combining unit operative to receive said processed digital signal and said second digital output signal and to combine both said signals into a final digital output signal;

whereby the analog-to-digital data conversion is at least partially performed in said frequency domain using spectral tools, thereby providing an improved dynamic range and quantization noise, a reduction or elimination of critical analog circuit

requirements and bottlenecks, and an increase of the sampling rate relative to existing Pipeline/Subranging architectures.

40. The method of claim 39, wherein said step of providing a first spectral signal processor operative to process said first digital output signals and other received digital signals in a frequency domain includes operating said first spectral signal processor to divide said frequency domain into at least two frequency domain parts, one said part related to a low-resolution signal to noise ratio (SNR) and another said part related to a high-resolution SNR, and to use said frequency information resulting from said dividing as an input in the obtaining of said output analog subtraction signal.